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ORIGINAL PAPER

Research on the application of digital power supply based on domestic FPGA

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Abstract

Purpose The digital controller for the accelerator magnet power supply typically employs a field-programmable gate array (FPGA) as the signal processing chip for executing digital processing of closed-loop control. Currently, FPGA chips are predominantly utilized in Intel or Xilinx products. To address the "key areas and stranglehold" issue pertaining to FPGA chips in accelerator power supply, we have devised a digital power supply prototype using a domestic FPGA chip and validated its feasibility in the upgrade project's magnet power supply digital transformation plan for the Beijing Electron Positron Collider (BEPCII).

Method A domestic FPGA chip from the Seal5000 SA5Z-30-D1 series by Xi'an ZhiDuoJing Microelectronics Co. serves as the core component for the design of a digital corrector magnet power supply to replace the existing analog controlled corrector power supply at BEPCII. The power supply's digital control of the closed loop is achieved through the use of a hardware description language, and the digital controller hardware is constructed based on the original power supply power topology.

Results and conclusions After conducting experiments and tests on the power supply prototype, we have successfully met the current operational requirements of the BEPCII corrector power supply, thus confirming the feasibility of utilizing domestic FPGA for digital application on accelerator power supply.

Keywords Domestic FPGA · Power supply digital controller of accelerator · PID algorithm · PWM

Introduction

The BEPCII corrector magnet power supply presently employs an analog control method. However, with the advancement of accelerator technology, there is a need for digitalization and localization of the magnet power supply. The digital switching power supply's control core is typically based on FPGA chips, which exhibit high parallelism and reconfigurability, meeting the design requirements of a mature system with algorithms to attain digital control. Currently, the primary digital controller chip utilized in accelerator power supply design involves imported chips. However, due to the US technology sanctions against China and the impact of the global new crown epidemic, FPGA chips have become scarce and costly, significantly increasing the digital controller's design cost [1–6].

To address the aforementioned issues, this paper proposes a digital application scheme for calibrating the power supply. It designs a digital controller with a domestic FPGA chip as the core and a firmware control program based on hardware description language to achieve the digital closed-loop control of the power supply, laying the foundation for using domestic signal processing chips to achieve digital control in the future.

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System architecture and principle

The power supply employed for this transformation is a ± 32 A/14 V bidirectional switching power supply with a switching tube operating frequency of 56.9 kHz. The conversion of AC power to DC is executed by a diode rectifier circuit, followed by voltage ripple reduction via a filter circuit. Electrical isolation and voltage conversion are achieved using a high-frequency transformer in conjunction with a classic H-bridge circuit featuring phase-shifted PWM (pulse width modulation) control. Finally, the bridge switching circuit is utilized as an electronic switch to realize the switching output of positive and negative directions.

Since the digital transformation of the power supply only involves the analog closed-loop control being changed to digital control, without altering the original structure of the power supply, the entire transformation is restricted by the original architecture while simultaneously considering the requirements of digital control. As shown in Fig. 1, the working principle of closed-loop control circuit topology involves the digital given signal being input to the FPGA chip through the rotary encoder after the power supply is activated. Subsequently, the feedback signal of the DCCT (direct-current current transformers) collected by the ADC (analog-to-digital converter) chip is input to the digital PID controller of the digital signal processor, which compares it with the given signal. The digital closed-loop algorithm compares the signals through the PID control algorithm to calculate the phase-shift PWM adjustment amount. This adjustment amount generates the corresponding PWM signal to control the MOSFET switching tube turn-on and turn-off time. Following several iterations of closed loop regulation, the accurate output current is ultimately attained [7–13].

Hardware circuit design

Domestic FPGA chip selection

As the core of the digital power supply controller, the hardware resources and performance of the FPGA chip will affect the stability of the final current output. Considering the first application of domestic FPGA chips in the digital transformation of BEPCII analog power supply, it is necessary to compare and evaluate the hardware performance of domestic FPGA chips with imported FPGA chips, in order to verify the feasibility of applying domestic FPGA chips to corrector power supply. After research, it has been found that the commonly used imported FPGA chips for accelerator digital power supply are mainly sourced from Intel and Xilinx, with Intel's Cyclone ® Taking the FPGA chip of the V 5CSEA 2 model as an example, the chip adopts a 28 nm process and contains 25000 LE (logic elements), 37736 register resources, 145 user I/O, and 1.538 Mb memory. The device integrates Single Arm * Cortex * - A9 or Dual core Arm * Cortex * - A9 and DDR controller embedded hard cores, but does not include embedded ADC hard cores. Taking the SA5Z30D18U213C of the Seal 5000 series from Xi'an Zhiduojing Company as an example of domestic

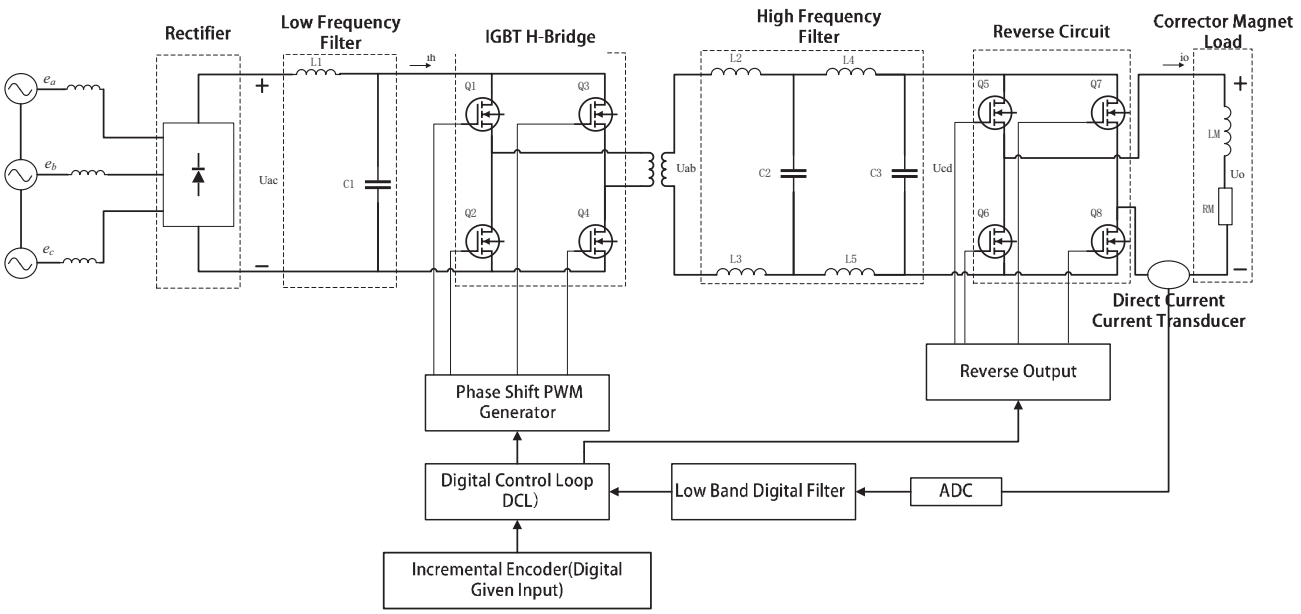

Fig. 1 Closed-loop control circuit topology

FPGA, the domestically produced FPGA chip also adopts a 28 nm process. The hardware resources include 32666 equivalent logic elements, 40832 registers, 243 user I/O, and 1.242 Mb storage resources. The embedded hardware core includes ARM, DDR2/3, and ADC controllers. The comparison of hardware resources between domestic FPGA chips and imported FPGA chips is shown in Table 1 [14, 15].

According to the comparison, it can be seen that compared to imported FPGA chips, domestic FPGA chips have hardware resources that meet the needs of transformation of power supply and have the same manufacturing process (28 nm). Considering that domestic FPGA chips have lower costs and shorter supply cycles, using domestic FPGA chips as power digital controller chips has certain feasibility. The controller core for transformation of power supply was chosen as the SA5Z30D18U213C FPGA chip from Xi'an ZhiDuoJing Microelectronics Co, which boasts a 28 nm process, LUT6 architecture, and integrated Cortex-M3 hard core, DDR2/3 hard core controller, 12-bit ADC, 124 Kbit DDR2 memory, and 1.2 Gbps LVDS. This highly integrated and cost-effective chip is suitable for a wide range of applications.

Table 1 Comparison table of domestic and imported FPGA hardware resources

FPGA chip model	Intel (Cyclone® V 5CSEA2 FPGA)	Xi'an Zhiduojing (SA5Z-30D18U213C)
Logic elements	25,000	32,666
Register	37,736	40,832
User I/O	145	243
Memory	1.538 Mb	1.242 Mb
ARM	Yes	Yes
DDR2/3 controller	Yes	Yes
ADC controller	No	Yes

Design of hardware framework for digital controller

The primary function of the digital controller in a switching power supply is to produce a stable phase-shifted PWM signal. Figure 2 shows the Design framework of digital controller main board, the main board design framework includes digital input and output interfaces for fault signal detection, power supply status detection, and remote-control state switching signal output, as well as an ADC chip to receive analog voltage signals from the DCCT and subsequent IV conversion. Four phases shifted PWM signal output interfaces are provided for switching tube duty cycle control, along with an Ethernet interface for OPI (Operator Interface) communication with the upper layer, and a serial port for FPGA development and debugging. The domestic FPGA core board design includes clock input, JTAG download interface, FLASH storage, and other expansion functions such as Ethernet and OPI communication.

Analog-to-digital conversion circuit design

The ADS8382B is an 18-bit high-precision analog-to-digital converter (ADC) chip with a sampling rate of up to 600 kHz. As depicted in Fig. 3, the ADS8382 AIN + and ADS8382 AIN-terminals are connected to the DCCT output, and the power supply's original DCCT output voltage varies between − 9.6 and + 9.6 V. The ADC is controlled

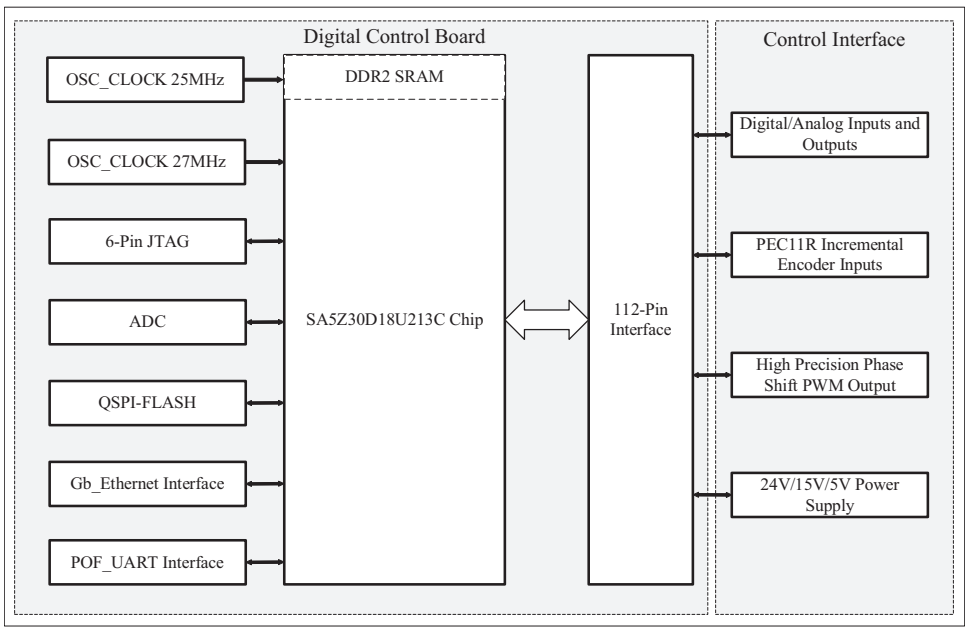

Fig. 2 Design diagram of digital controller main board framework

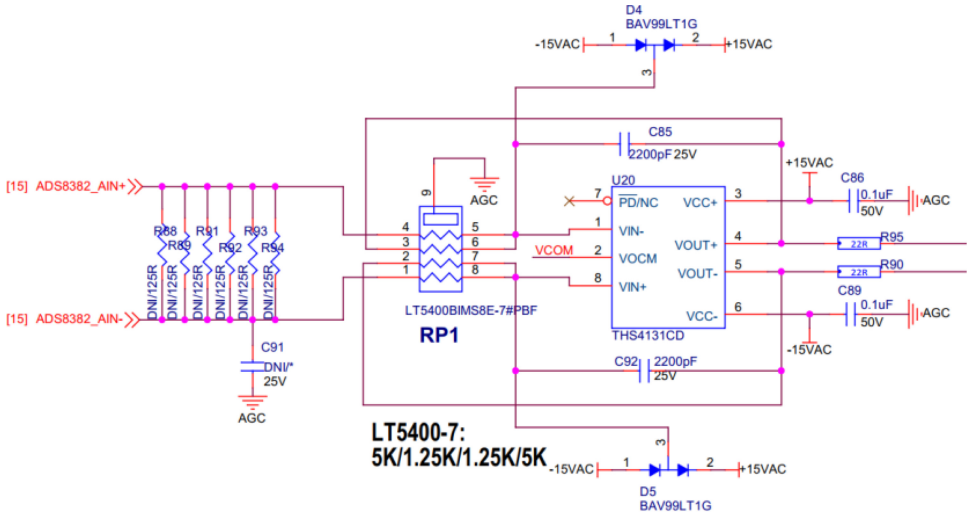

Fig. 3 Schematic diagram of ADS8382 front-end circuit design

using a reference voltage of 2.5 V, and the output signal is adjusted through the front-end 4:1 precision electric compression ratio control and precision differential operational amplifier to comply with the input voltage range requirements of the ADS8382. As shown in Fig. 4, the chip select signal *CS* and the reset signal *PD* port are grounded, which allows the chip to maintain the maximum conversion rate and improve the overall computation speed of the system. The ADC's theoretical resolution can reach $1/2^{18}$. Despite the system's primary frequency being 50 MHz, it can achieve 100 MHz through PLL circuit for closed-loop algorithm processing, and the PWM regulation accuracy can be improved by combining PWM and PFM, which is equivalent to digital averaging method to improve the resolution, fully meeting the power supply control requirements.

Digital input and output circuit design

The digital input and output signals and PWM signals are electrically isolated by optocouplers. The design schematic diagram of optocouplers is shown in Fig. 5.

Control program design

Design the FPGA control program using the Verilog hardware description language, according to the function of the digital control board. Figure 6 shows the framework of control program, the control program effectively addresses several critical issues, namely: (1) Fault detection, fault protection, and reception of power status quantities, as well as switching and remote control switching logic; (2) Processing

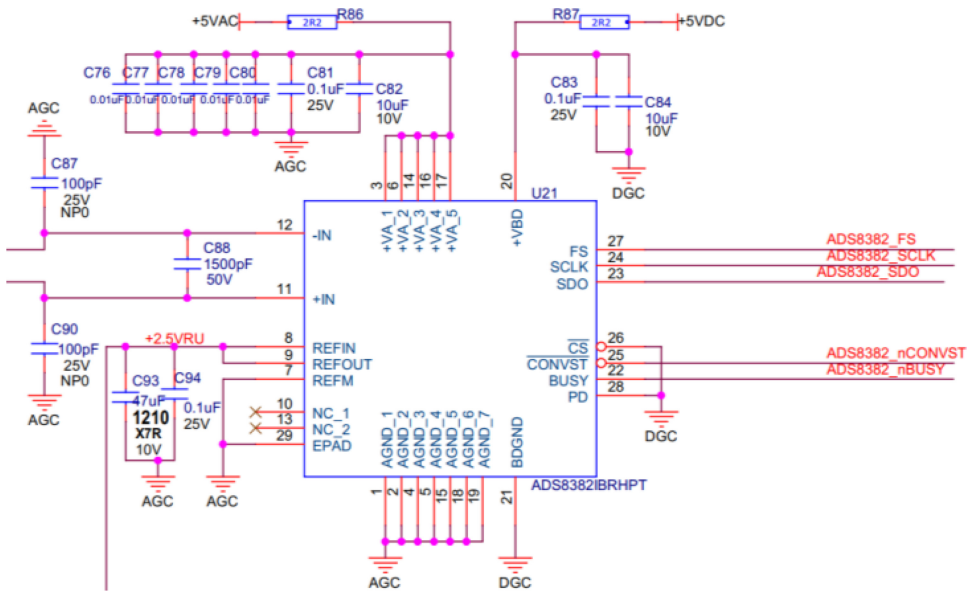

Fig. 4 Schematic diagram of ADS8382 chip peripheral circuit

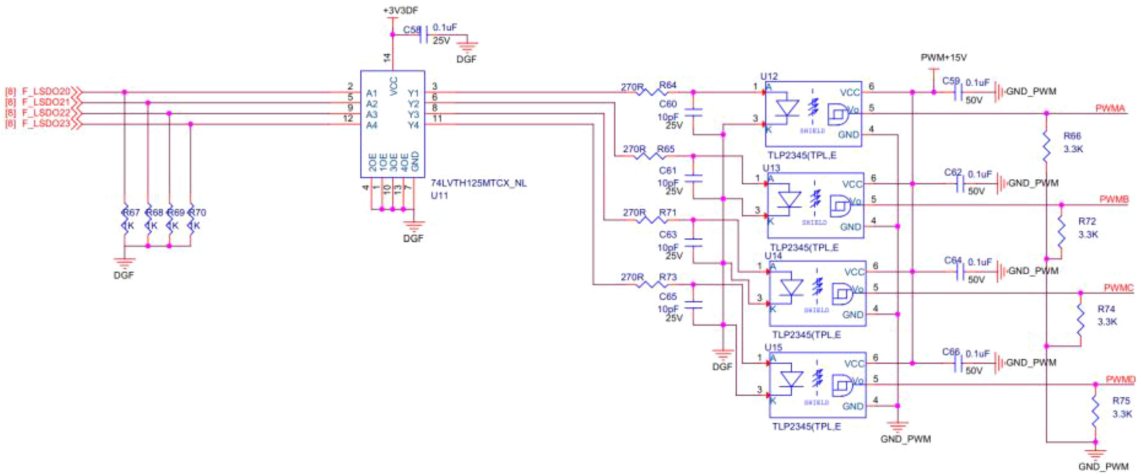

Fig. 5 Optocoupler isolation circuit schematic

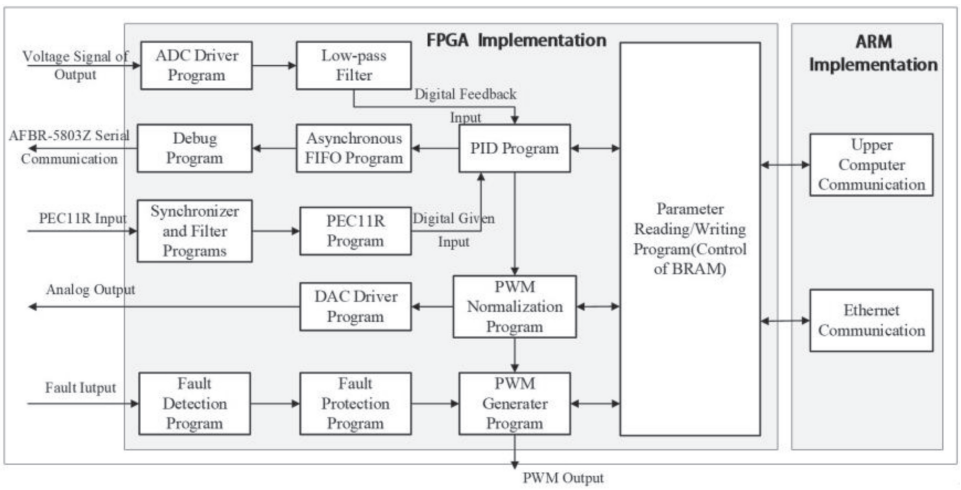

Fig. 6 Framework of control program

of PEC11R rotary encoder input signals and generation of ADS8382 chip drive signals; (3) Generation of 4-way phase-shift PWM control signals, and control of the power topology of the switching tube drive circuit; (4) Utilization of a PID automatic control algorithm to form a closed-loop system that enhances current control accuracy and stability, specifically in the face of two different sources of disturbance—grid fluctuations and load temperature changes.

Incremental encoder program implementation

According to Fig. 7, it can be seen that based on the operational principle of the incremental encoder PEC11R, a continuous square wave signal is produced at the output. The initial step requires synchronizing the signal, filtering out the spurious signal, and subsequently describing the phase behavior of the filtered signal. The second step entails detecting the rising edge of phase A-C, while

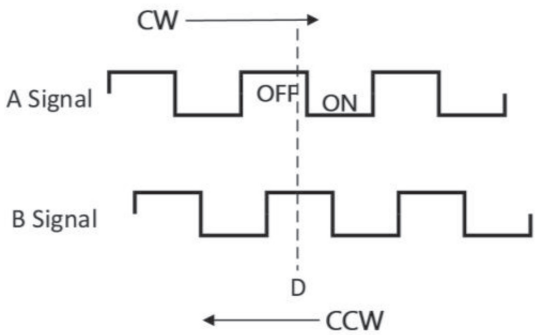

Fig. 7 PEC11R working principle

simultaneously monitoring the phase B-C level. If B-C is low, PEC11R is deemed to be in forward rotation; and conversely, if the level is high, the encoder is deemed to be in reverse rotation. The third step involves detecting

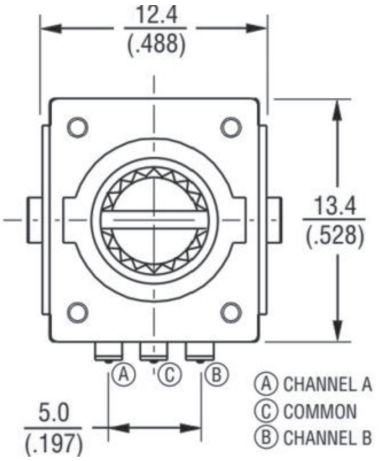

Fig. 8 PEC11R structure diagram

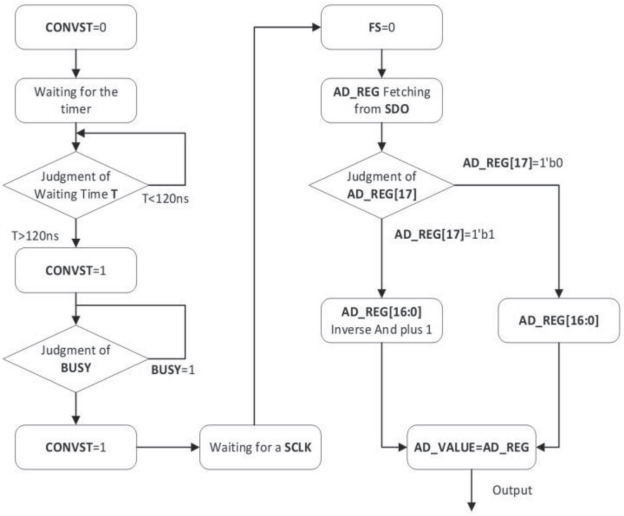

Fig. 9 ADS8382 program flowchart

Table 2 ADS8382 chip control signal

Pin	I/O	Function
CS	I	Chip selection signal
COVST	I	Low level indicates the start of conversion
FS	I	Chip Frame synchronization signal
SCLK	I	Serial data driven clock
SDO	O	Serial data output
PD	I	High level chip reset signal
BUSY	O	High level means conversion is in progress

the falling edge of A-C phase. If B-C is high, the positive rotation is deemed to be completed, and the totalizer is incremented by "1". Conversely, if the level is low, the reverse rotation is deemed to be completed, and the totalizer is decremented by "1". The output value of the totalizer serves as an input to the PID algorithm, which employs it as the setpoint signal for further operation. Figure 8 shows the structure diagram of PEC11R.

ADS8382 driver implementation

As shown in Table 2, the ADS8382 drive signal comprises of five input signals and two output signals. In order to ensure that the chip operates at its maximum conversion rate, the chip select signal (CS) and the high-level reset signal (PD) have been grounded during the circuit design. The remaining signals are required to be generated or processed by the FPGA. Figure 9 shows the program flowchart of ADS8382, according to the description in the figure, the specific design process involves the initial step of pulling the CONVST signal low, following which, it is pulled high after a low level that lasts for 120 ns. This signifies that the chip has entered the analog-to-digital conversion stage, and the BUSY signal is high. In the second step, the BUSY signal is checked to determine if it is low. If so, it indicates that the analog-to-digital conversion is completed, following which, the frame synchronization signal (FS) is pulled high. After a duration of SCLK, FS is pulled low. In the third step, the digital quantity obtained through the conversion is read by SDO. Subsequently, the CONVST signal is pulled low for the next conversion. The drive signal is captured using GTKwave, and the result is depicted in Fig. 10. The calculation verifies that the ADC accurately detects the signal [16].

Implementation of the PID algorithm program

The implementation of the PID algorithm program is a conventional algorithm in automatic control theory, Fig. 11 shows the PID schematic diagram. Practical application has confirmed that the PID algorithm is effective in controlling accelerator power supply. In the digital system, the PID algorithm is transmitted in the form of discrete time signals. It is known from knowledge of digital signal processing that a certain discrete method can be obtained after continuous PID control, which leads to digital PID control. The essence of discrete is signal sampling, and the algorithm is periodically sampled with a sampling period of T. The independent variable of the discrete PID algorithm is n. According to the positional PID control formula, the control amount at the $n-1$ moment of the discrete time domain PID algorithm can be expressed.

$$u[n-1] = K_{\mathrm{p}}\{e[n-1] + \frac{T}{T_i}\sum_{i=0}^{n-1} e[i] + \frac{T_{\mathrm{d}}}{T}\{e[n-1] - e[n-2]\}\} \tag{1}$$

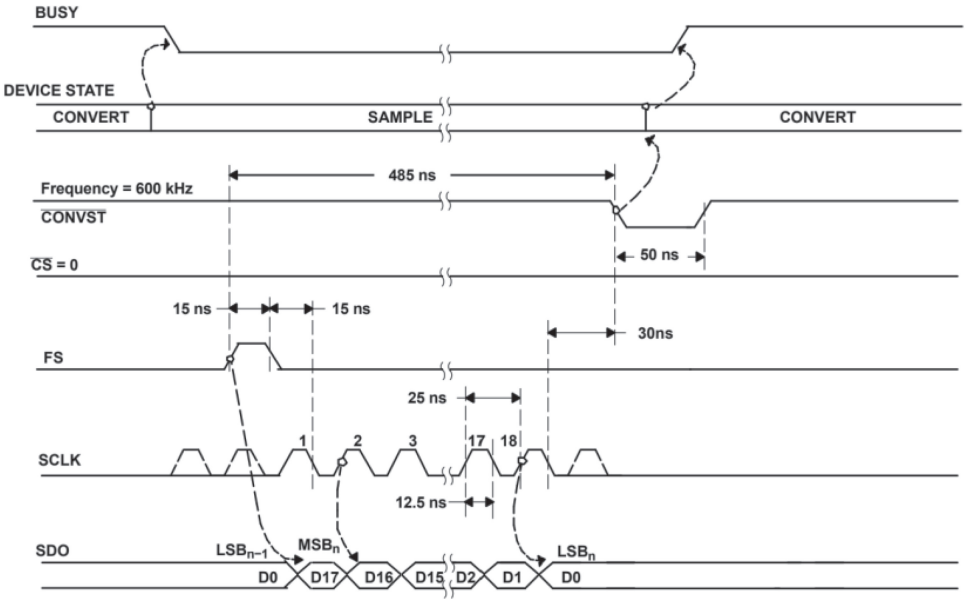

Fig. 10 ADS8382 drive signal waveform

If,

$$\Delta u[n] = u[n] - u[n-1] \tag{2}$$

Then,

$$\begin{aligned}\Delta u[n] = K_p\{e[n] - e[n-1]\} + \frac{K_p T}{T_i} e[n] \\ + \frac{K_p T_d}{T_i}\{e[n] - 2e[n-1] + e[n-2]\}\end{aligned} \tag{3}$$

Assuming that $K_i = K_p T/T_i$ and $K_d = K_p T_d/T_i$ are the integral and differential coefficients, respectively, the aforementioned equation can be streamlined as follows.

$$\begin{aligned}\Delta u[n] = K_p\{e[n] - e[n-1]\} + K_i e[n] \\ + K_d\{e[n] - 2e[n-1] + e[n-2]\}\end{aligned} \tag{4}$$

The PID module in the analog controller consists of a differential operational amplifier circuit, which is depicted in Fig. 12. The values of the components are $R = 100$ kΩ, $R_f = 33$ kΩ and $C_1 = 1$ uF. The given voltage is set as u_{i1}, and the return voltage is set as u_{i2}. According to the "virtual short" and "virtual open" principle, set $u_p = u_n$, and C_2 is the filter capacitor. Its role is to prevent high-frequency component amplification saturation, which can be ignored in the calculation. The Kirchhoff's law is applied.

$$i_1 = i_{f1} = \left(u_{i1} - u_p\right)/R_{i2} \tag{5}$$

$$i_2 = i_{f2} = \left(u_{i2} - u_n\right)/R_{i2} \tag{6}$$

$$u_n - u_{o1} = i_{f2} R_f + \frac{1}{R_f C_f}\int i_{f2} \tag{7}$$

$$u_p = i_{f1} R_f + \frac{1}{R_f C_f}\int i_{f1} \tag{8}$$

Substituting the above equation gives

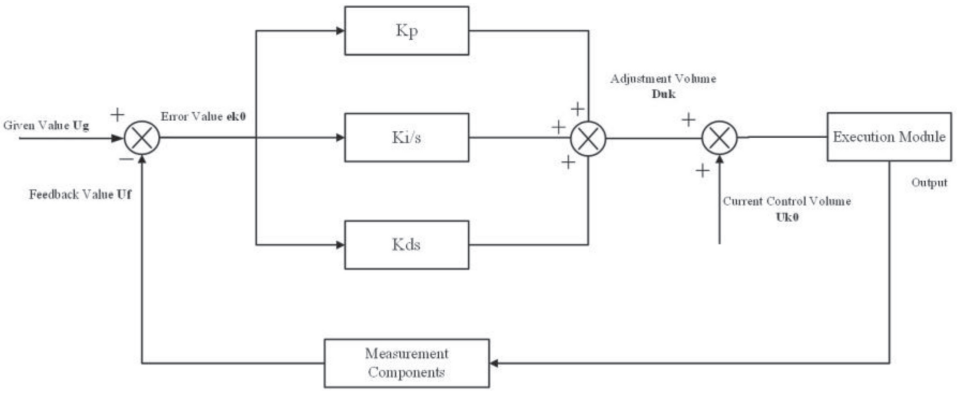

Fig. 11 PID schematic

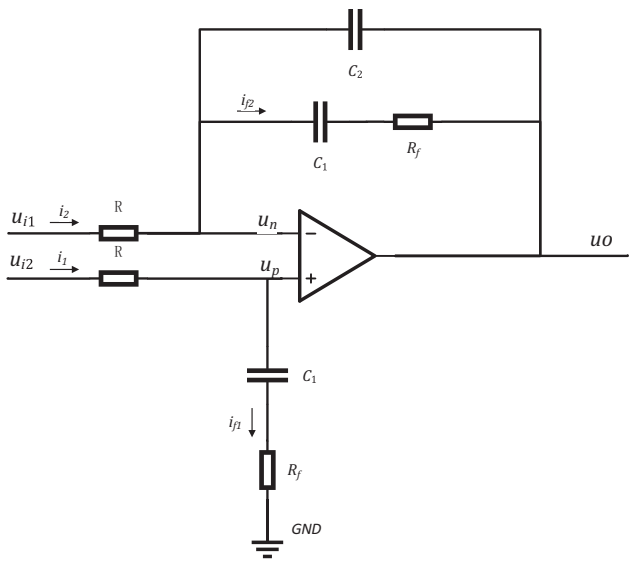

Fig. 12 Analog PID controller

$$u_o = R_f i_{f1} - i_{f2} + \frac{1}{R_f C_f} \int i_{f1} - i_{f2} \tag{9}$$

According to formula (1)–(9), the parameters of the PID algorithm are calculated $K_p = 0.333$ and $K_i = 10.000$. In the program design, the PID parameters are designed with reference to this design index, and the parameters are optimized according to the relevant theory and experimental results. The multiplier resources and PLL resources in the FPGA chip DSP are called to build the PID algorithm module. As shown in Fig. 13, the design method is as follows: in the first step, the input given signal and the feedback signal are compared to generate the error signals ek0, ek1, and ek2. Where ek0 is the current moment error signal, and ek1 and ek2 are the previous two moments' error signals. In the second step, the proportional, integral, and differential modules are multiplied and finally summed up as the regulation output. Since the multiplier currently supports only fixed-point operations, the design is commented and recorded for the fixed-point integer and decimal bits of each signal. The specific implementation flow is shown below. The algorithm adopts a pipeline design to cache the calculated regulation data in the buffer and update the regulation amount when the next rising edge of the clock comes, so as to realize the dynamic regulation of the current value.

System test

Performance assessments were executed on the magnet power provision prototype, employing a 0.5 Ω resistive load. The experimental prototype of the power supply was assembled as per the power supply topology schematic, and the platform for assessing current stability was constructed. Figure 14 showcases the experimental prototype of the power supply subsequent to the installation of the digital controller. Domestic FPGA digital controller (1), inverter bridge board (2), DCCT (3), auxiliary board (4), filter board (5), and fan (6) constitute the prototype, as seen in the aforementioned figure. Figure 15 illustrates the present test platform. Upon transformation of the output current of the prototype power supply by the DCCT, the closed-loop voltage value is examined through employment of

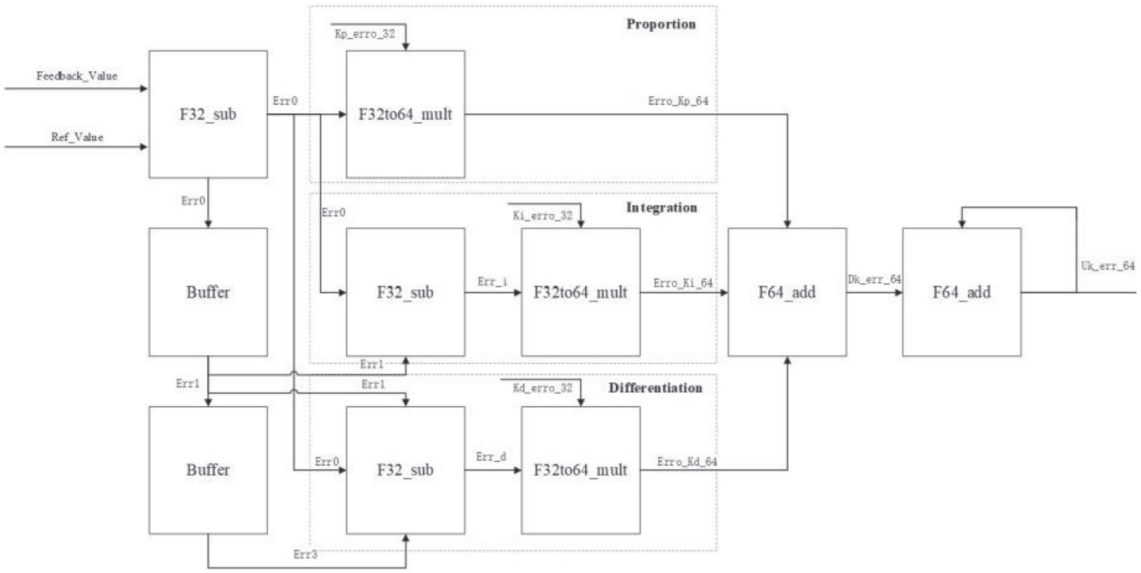

Fig. 13 PID algorithm program implementation flowchart

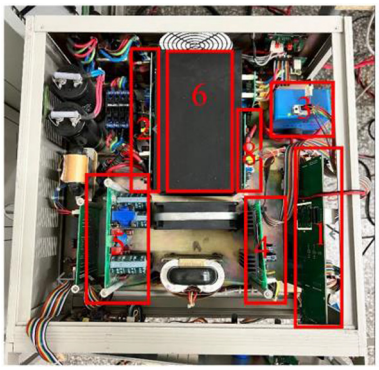

Fig. 14 Corrector magnet power supply experimental prototype

Fig. 15 Current stability test platform

a six-and-a-half-digit voltmeter, and the current stability is collected and analyzed by the upper computer program.

Current stability and voltage ripple measurement

The current stability and voltage ripple can be defined as follows:

$$S = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \tag{10}$$

S represents the current stability, where I_{max} and I_{min} denote the maximum and minimum values of current fluctuation, respectively, during the test.

$$V_r = \frac{V_{p-p}}{V_o} \tag{11}$$

V_r signifies the output voltage ripple, where V_{p-p} represents the peak-to-peak value of the output voltage fluctuation, and V_o denotes the output DC voltage value during testing.

The power supply controller established the current value at 8.014 A, and the measured current data recorded a maximum value of 8.014497 A and a minimum value of 8.0137736 A. Subsequently, the current stability was computed and amounted to 43 ppm (Fig. 16). According to Figs. 17 and 18, the high-frequency noise voltage is 6 mV and the low-frequency noise voltage is 2 mV. After calculation, the voltage ripple value is 3×10^{-3} when the measured output DC voltage value is 4.007 V. It is worth noting that both the current stability and voltage ripple satisfy the performance requirements of the corrector power supply.

Conclusion

This paper explores the feasibility of employing domestic FPGA chips as the primary control chip for the accelerator magnet power supply in response to foreign technology sanctions and the "key areas and stranglehold" problem. The results of the prototype testing indicate that the domestic FPGA chips have a lower cost, shorter procurement period, and stable supply and performance in comparison to the Altera FPGA chips. To meet the digital transformation

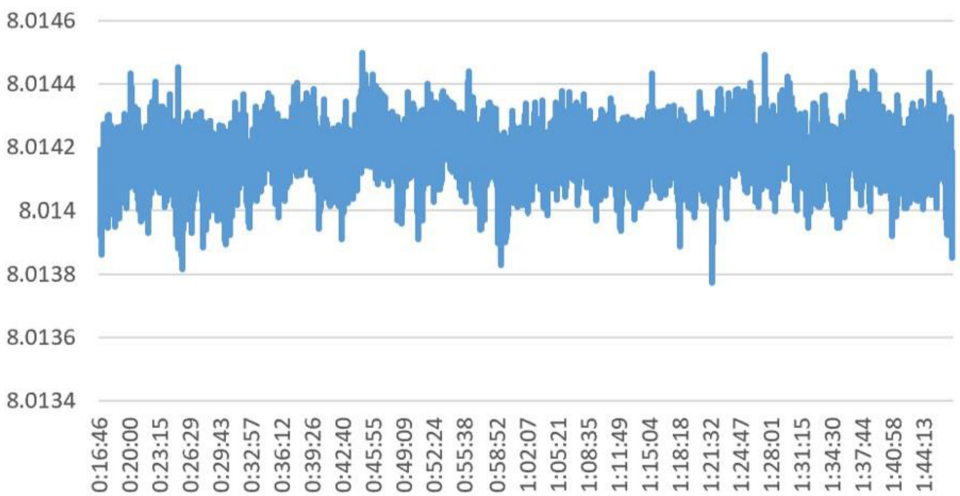

Fig. 16 Current waveform of current stability

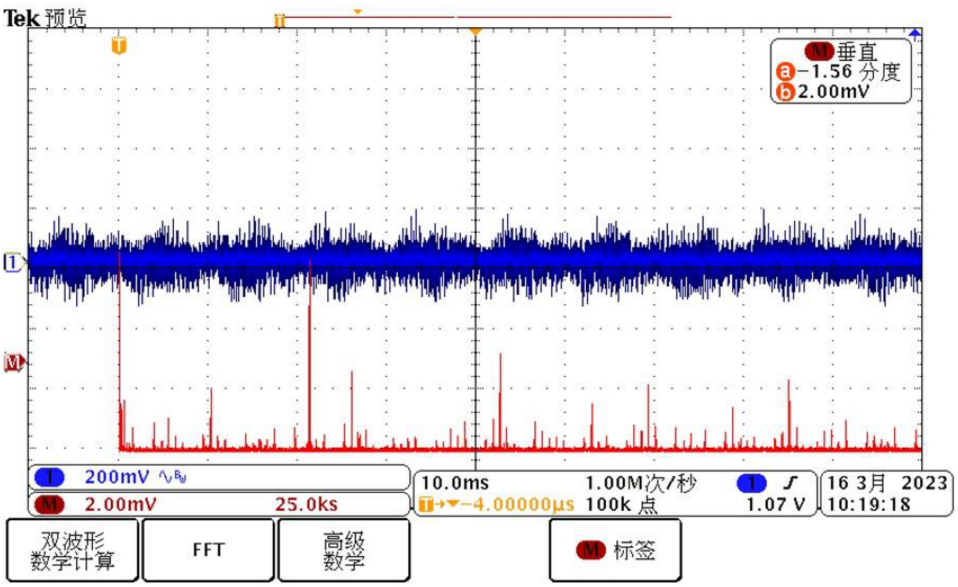

Fig. 17 High frequency voltage ripple test

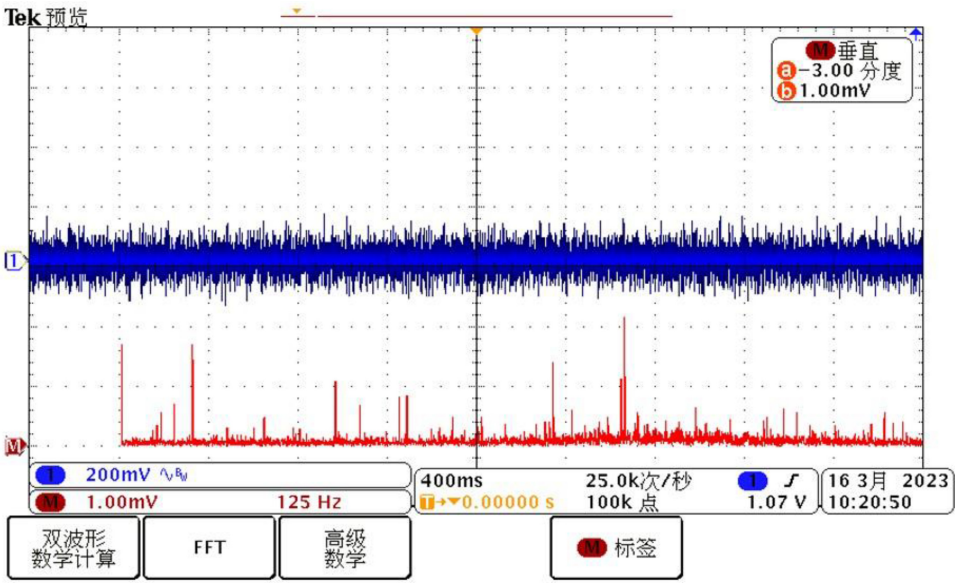

Fig. 18 Low frequency voltage ripple test

requirements of the corrector power supply, this paper develops a digital controller with the domestic FPGA as the core and completes the program design. The feasibility of the digital transformation of the domestic FPGA into an accelerator power supply is verified through prototype testing, and the experimental results meet the operational requirements of BEPCII. This lays a solid foundation for the digital control of the domestic chip of the accelerator power supply and validates the feasibility of using domestic FPGA as the control chip of the accelerator power supply.

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Declarations

Conflict of interest We declare that we have no conflict of interest in this article.

References

1. S. Chen, M. Zhan, F. Long, W. Ye, Development of rapid detection system on bepcii magnet power supply. Atom. Energy Sci. Technol. **48**(11), 2123 (2014)
2. X. Wang, P. Liu, F. Long, W. Su, Y. Gao, X. Shi, T. Zeng, G. Wu, J. Cheng, Design of control algorithm for accelerator magnet

power supply with large time constant load. Radiat. Detect. Technol. Methods **4**, 383–391 (2020)
3. Y. Li, Q. Zhou, P. Liu, J. Zhang, F. Long, Simulation for accelerator dynamic power supply based on current-source pwm rectifier. Radiat. Detect. Technol. Methods **2**, 1–7 (2018)
4. Q. Xin, Z. Jing, H. Zuyue et al., Magnet power supply system for china spallation neutron source. Power Electron. **2014**(12), 14–16 (2014)
5. X. Qi, Z. Xu, et al., Resonant magnet power supply system for the rapid cycle synchrotron of Chinese spallation neutron source, in *Proceedings of APAC, Gyeongiu, Korea* (2004)
6. P. Yang, J. Xu, S. Zhang, J. Wang, Peak current control mode for quadratic boost converter. Diangong Jishu Xuebao Trans. China Electrotech. Soc. **26**(5), 101–107 (2011)
7. K. Sugita, E. Fischer, H. Khodzhibagiyan, H. Muller, J. Macavei, G. Moritz, Design study of the multipole corrector magnet for sis 100. IEEE Trans. Appl. Superconduct. **19**(3), 1154–1157 (2009)
8. G.O. Brunheira, J.P. Bonaldo, J.N.H. Rosa, C. Rodrigues, J.A. Pomilio, Digital control system for high precision power supplies of the new brazilian synchrotron source, in *2013 Brazilian Power Electronics Conference*, pp. 326–331 (IEEE, 2013)
9. Y. Kurimoto, Y. Morita, S. Nakamura, T. Shimogawa, Precise current control in accelerator magnets with a digital feedback system. IEEE Trans. Nucl. Sci. **61**(1), 546–552 (2014)
10. H. Chen, R. Li, C. Guo, T. Shen, D. Li, An innovational application of digital power supply controller on ssrf dynamic power supply. Nucl. Tech. **31**(10), 726–730 (2008)
11. X. Wu, C. Wang, J. Wang, J. Liu, Y. He, The design and implementation of the remote control of a digital power supply control module based on modbus/rs232. Nucl. Electro. Detect. Technol. **32**(8), 867–870 (2012)
12. J. Ding, H. Zhao, H. Zhu, Y. Liu, L. Shen, The ssrf power supply control system. Nucl. Tech. **35**(8), 573–577 (2012)
13 K. Zhao, W. Liu, Q. Mu, H. Wang, R. Li, Z. He, Pcie cryptographic accelerator based on domestic fpga, in *2022 International Conference on Computing, Communication, Perception and Quantum Technology (CCPQT)* (IEEE, 2022), pp. 25–31
14. Hardware Resource Table of Xi'an Zhiduojing Seal 5000 Series FPGA, isilicontech.com
15. Hardware Resource Table of Intel Cyclone V Series FPGA Chip, Cyclone® V 5CSEA2 FPGA (intel.cn)
16. Datesheet of ADS8382, ADS8382 data sheet, product information and support, TI.com